

PATENT APPLICATION

Sheet 1 of 2

FORM PTO-1449		ATTY. DOCKET NO. 200310231-1	APPLICATION NO. 10-735549	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		APPLICANT Herbert R. KOLK et al.		
(Use several sheets if necessary)		FILING DATE Herewith	GROUP	2826

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
1A				
1B				
1C				
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1J				
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

NMD	1Q	Lesley POLKA et al., "Package-Level Interconnect Design for Optimum Electrical Performance," Intel Technology Journal Q3, 2000, pp. 1-17.
NMD	1R	George A. Riley, "Picking Your Flipchip: A Comparison of Flipchip Methods and Benefit," 6 pp. [online] http://www.flipchips.com/SMErev01.htm .
NMD	1S	"Calculating the Number of Bumps Needed," 15 pp. [online] http://www.artwork.com .

EXAMINER

DATE CONSIDERED

10/06/05

PATENT APPLICATION

Sheet 2 of 2

FORM PTO-1449		ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
		200310231-1	10235599	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		APPLICANT		
(Use several sheets if necessary)		Herb rt R. KOLK et al.		
		FILING DATE	GROUP	
		Herewith	02826	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

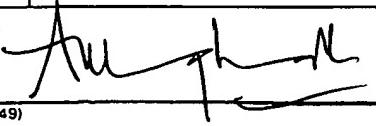
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1L					
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1N					
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1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

NMD	1Q	"Die-Bump Designer Suite," CAD Design Software, 4 pp.
	1R	
	1S	

EXAMINER  DATE CONSIDERED
10/16/10